Model Group			SX-ACE							
Node	Processor									
	Architecture		4-core vector processor							
	Logical Peak Performance *1		276GFLOPS (69GFLOPS x4core)							
	Peak Vector Performance *2		256GFLOPS (64GFLOPS x4core)							
	Vector Register		2KByte x72/core							
	Scalar Register		64bit x128/core							
	Memory									
	Memory Capacity		64GByte							
	Peak Memory Transfer Rate		256GByte/sec							
	Input/Output									
	Number of Max Channels		16							
	Peak Data Transer Rate		8GByte/sec x2 (bidirectional)							
System	Configuration									
	Number of Nodes		64	128	192	256	320	384	448	512
	Performance									
	Logical Peak Performance (TFLOPS) *1		17.7	35.3	53.0	70.7	88.3	106.0	123.6	141.3
	Peak Vector Performance (TFLOPS) *2		16.4	32.8	49.2	65.5	81.9	98.3	114.7	131.1
	Memory									
	Memory Capacity (TByte)		4	8	12	16	20	24	28	32
	Peak Memory Transfer Rate (TByte/sec)		16.4	32.8	49.2	65.5	81.9	98.3	114.7	131.1
	Input/Output									
	Number of Max Channels		128	256	384	512	640	768	896	1,024
	Peak Data Transer Rate (GByte/sec)		512	1,024	1,536	2,048	2,560	3,072	3,584	4,096
	Interconnect									
	Topology between Nodes		2-stage fat-tree							
	Peak Data Transer Rate between Nodes	1 lane	4GByte/sec x2 (bidirectional)/node							
		2 lane	8GByte/sec x2 (bidirectional)/node							
	Implementation									
	Cabinet Size (WxDxH in mm)		Node cabinet 750×1,500×2,000 Interconnect cabinet 1,850×1,150×2,000							
	Number of Node Cabinets		1	2	3	4	5	6	7	8
	Number of IXS Cabinets	1 lane	1							
		2 lane	1					2		
	Cooling Method		Hybrid cooling (water and air)							

*1:Peak performance includes the theoretical operation rate of the vector add, multiply, divide, and square root units as well as the scalar unit.
*2:Peak vector performance is traditionally based on the multiply and add vector units.

Safety Notice	Before using this product, please read carefully and comply with the cautions and warnings in manuals such as the Installation Guide and Safety Precautions. Incorrect use may cause a fire, electrical shock, or injury.

For further information, please contact:

NEC Corporation As of October 2013 Cat.No.E11-13090003E

Empowered by Innovation NEC

Vector Supercomputer SX Series

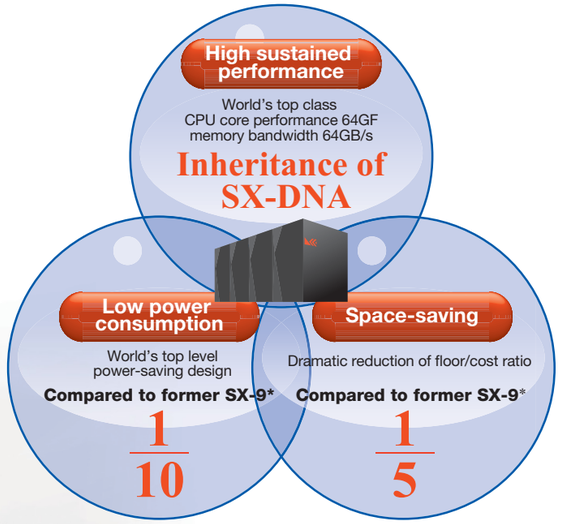
SX-ACE®

NEC SX-ACE:
Achieving an unprecedented stage beyond the stereotype of supercomputers

SX-ACE

Top class supercomputing based on industry-leading specifications combined with an environmentally friendly design

Currently, there are various kinds of issues on the earth. The complicated and large-scale issues need to be solved as efficiently and quickly as possible, and social environment which people can live safely beyond the differences of countries or regions needs to be created. NEC vector supercomputer SX series have continued to improve dynamically as the most advanced research tool in various fields and contributed problem-solving all over the world since the first release in 1983.
The new SX-ACE is a next generation supercomputer which inherits SX-DNA and achieves world's top class CPU core performance and memory bandwidth. In addition, the SX-ACE employs the most advanced design philosophy targeting environmentally friendly operation, such as excellent power-saving and space-saving at the same time.
Towarding an information society friendly to humans and the earth, NEC provides the best answer with the development of the SX-ACE.

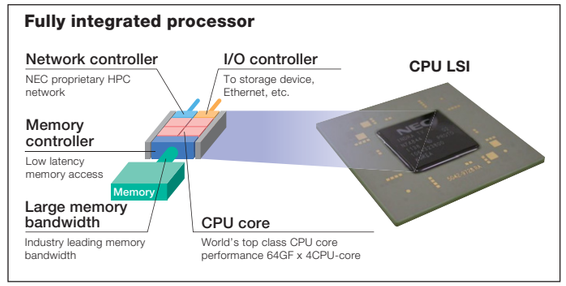


*Compared to former SX-9 with the same performance

The continuation of the NEC SX vector architecture targeting environmentally friendly supercomputing

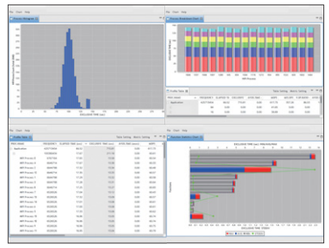
Similar to its predecessors, the SX-ACE provides outstanding computational efficiency and consequently high sustained performance. Together with excellent usability, the system provides real value to the scientists and engineers. The design is targeting very low power consumption and dramatically reduced floor-space requirements.
The CPU integrates four vector-cores with in total 256 GFLOPS*1 of peak performance and all interfaces. The computational efficiency is achieved by the unrivaled bandwidth to memory of 256 GB/s per CPU and by the latency-hiding effect of the vector architecture. The multi-node system connected by a proprietary interconnect can deliver excellent performance. NEC provides the next generation supercomputing environment to customers as the most advanced research tool.

*1:Giga Floating-point Operations Per Second



Realizing high reliability, high scalability, and high usability

The operating system of the SX-ACE is "SUPER-UX". It extracts the maximum hardware performance of the high performance vector cluster. It is equipped with powerful and flexible functionalities necessary for next generation supercomputing, such as the support of the new high capacity and high performance file system and large scale multi-node systems. Moreover, the SX-ACE handles all prevailing programming models of vector processing and parallel processing. Libraries and tools necessary for scientific and engineering applications and software development are available.



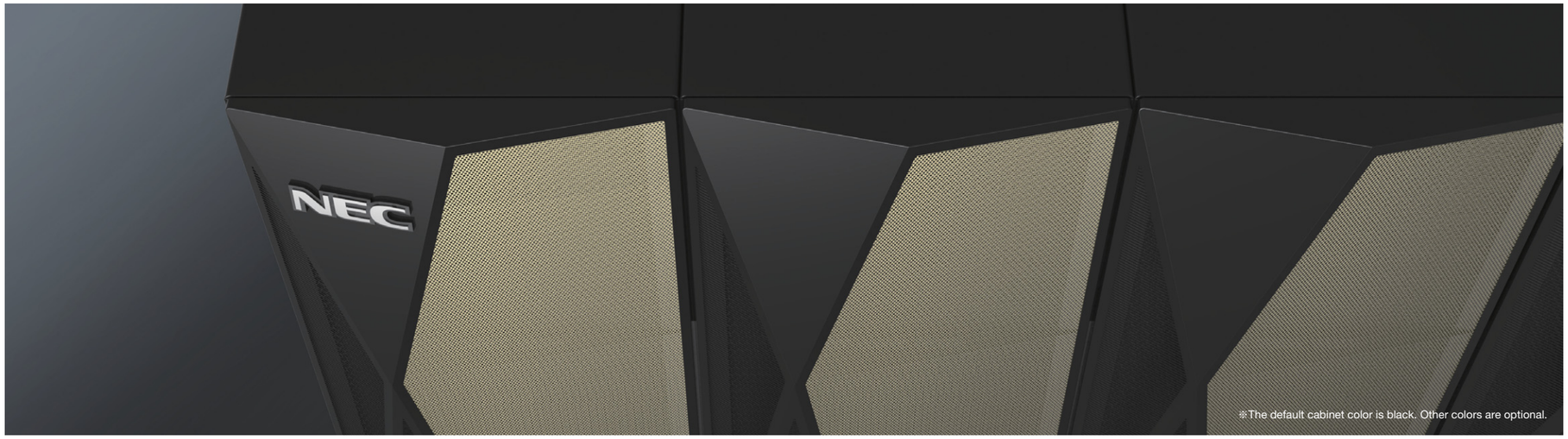
Ftrace Viewer

Green supercomputing by power-saving technologies

A significant reduction of the power consumption and floor space are the dominating design targets of the SX-ACE. To achieve this goal, the processor fully integrates all necessary interfaces like memory-, network- and IO-controllers. Together with the usage of advanced LSI-technologies, the power consumption of the system is a factor of 10 lower than a comparable configuration of an SX-9, and the floor space requirement is a factor of 5 smaller. The software is supporting the green supercomputing even further by advanced features of the scheduler and additional precautions for power-saving.

Targeting high sustained performance and efficiency in all respects to address the increasing needs of science and engineering

The SX design philosophy aims to provide high performance and usability to customers continuously. In order to achieve this goal, NEC sticks to high single-core performance and leading technology for high memory bandwidth. Common serious problems of modern computer systems, increasingly not only in the HPC field, are the so-called "memory wall" and "power wall". The problems are caused by a lack of memory bandwidth and power limitations. The SX-ACE overcomes these limitations and provides high performance and effective supercomputing environment to users.



※The default cabinet color is black. Other colors are optional.

Well balanced high performance I/O configuration

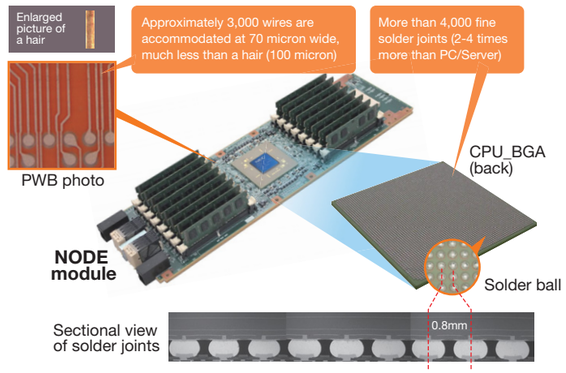
The real world applications consistently show that I/O performance is becoming increasingly important. In order to address this need, the I/O is highly integrated with the SX-ACE CPU. That way a single node can achieve I/O performance of up to 8 Gbyte/s per processor LSI.

SX-ACE architecture and technology

The SX-ACE is the only architecture targeted for the most demanding HPC applications. Its processor builds upon the successful history of the SX product line, achieving higher memory bandwidth by the integration of the memory controller on the chip. The CPU is implemented using the most advanced technologies, such as 28nm CMOS LSIs and 11-layer copper wiring. By these 256 GFLOPS of peak performance and 256 GB/s of memory bandwidth per processor are achieved.
Furthermore, an outstanding power efficiency is achieved by adopting the most advanced technologies, such as 10 Gbps-SerDes, Multi-Vth transistor, clock gating per register/CPU core unit, and power voltage optimizer.

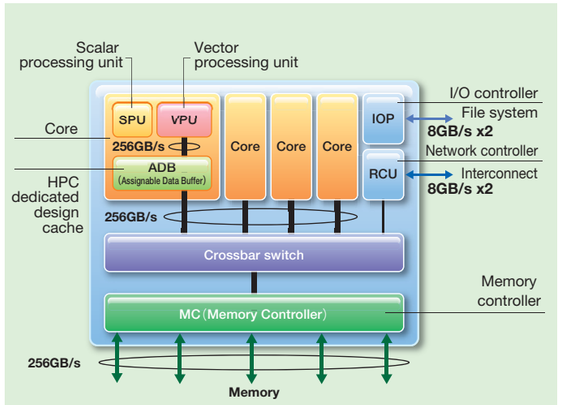
Highly scalable multi-node system

In the SX-ACE, data communication between nodes can be accelerated, and high performance and high scalability in parallel processing are achieved by the network communication controller in the processor LSI. The nodes of the SX-ACE are connected by a highly scalable proprietary interconnect, the IXS. It implements the topology of a full non-blocking fat tree with a link bandwidth of 8 GByte/s per direction. With the standard 2 level fat tree network, a multi-node system can be easily configured. That way highly scalable HPC environment by large scale shared/distributed memory system can be built.



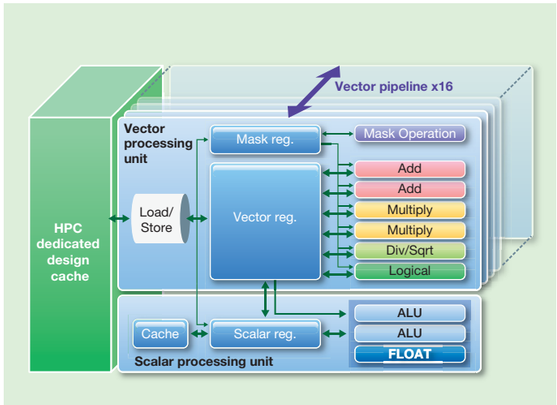
Environmentally friendly SX-ACE fully integrated processor with high sustained performance

The SX-ACE is using the world's only real vector architecture core with a large vector cache specifically designed for supercomputing usage. The 4-core vector processor is fully integrated with the memory and network interface controllers on one single LSI to ensure highest efficiency at lowest power-consumption for environmentally friendly supercomputing.



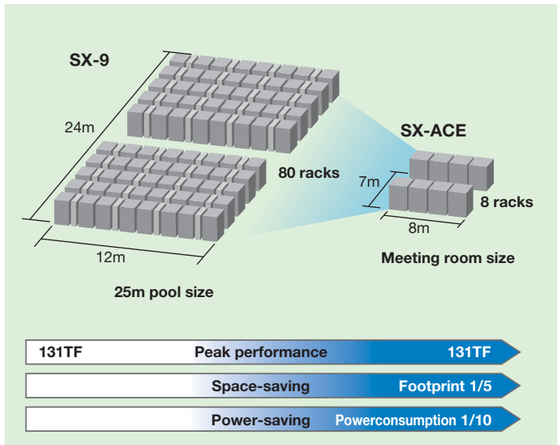
World-leading CPU core performance and memory bandwidth

Different from synthetic benchmarks, real relevant applications exhibit limited scalability. To overcome these limitations and to provide high sustained performance and usability, NEC continues the vector architecture with a strong single core performance of 64 GFLOPS and a high memory bandwidth of 64 GB/s per core. That way users can achieve the necessary real application performance even if the code requires a lot of memory bandwidth and does not scale perfectly well.



Significant reduction of the power consumption and floor-space requirement

The number of LSIs for an SX-ACE configuration is reduced by a factor of 100 compared to an SX-9 configuration with the same performance. As a result, a configuration based on the SX-ACE requires a factor of 10 less electricity and a factor of 5 less space than a SX-9 configuration with the same performance.



RAS-features of the SX-ACE

Compared to the SX-9, the number of parts of a node is drastically reduced by the fully integrated LSI, and consequently achieves a very high reliability. NEC is attempting to improve reliability and availability by adopting various kinds of leading technologies.
The memory architecture uses error correction codes (ECC), error detection functions are implemented on the processor LSI, and a built-in diagnosis (BID) makes sure that faults are recognized and then a reconfiguration is carried out. All information is automatically logged and provided to the service center of NEC for reaction. That way the reliability, availability, and maintainability of the system are increased, and the customers' operations are ensured for their business needs.

Work effectively: an operationally proven user environment for the success of scientists and engineers

The operating system of the SX-ACE is the SUPER-UX, a production-proven environment based on UNIX System V with a lot of extensions for performance and functionality. It has been further developed to include the new high performance and high capacity file system, to scale to a huge number of nodes, and to support the efficient utilization of the SX-ACE architecture. The SX-ACE handles all prevailing programming models of vector processing and parallel processing. Libraries and tools necessary for scientific and engineering applications and software development are available.

Distributed/Parallel File System	NEC Scalable Technology File System (ScaTeFS)
Resource Management	NQSII
Job Scheduling	JobManipulator
Software Development Environment	Fortran/C/C++ Compiler
	MPI library
	HPF/SX V2
Software Development Aid Tool	NEC Ftrace Viewer
	NEC Remote Debugger
Scientific Computing Library	ASL
	ASLSTAT
	MathKeisan
Operating System	**SUPER-UX**

※The default cabinet color is black. Other colors are optional.

Operating system, "SUPER-UX"

The SUPER-UX provides a user environment adhering to the common protocol standards, such as TCP/IP, DNS*2, and SNMP*3. It also provides POSIX conformance system call (2008 Edition partially conformed) for high portability and operability.

● Multi-node support

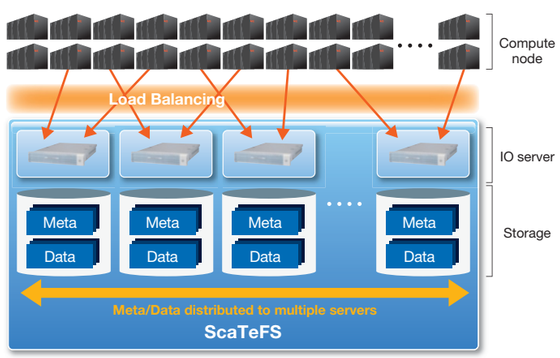
Even the biggest SX-ACE system such as hundreds of nodes provides a single system image to both users and system administrators for effective usage.

*2: Domain Name System *3: Simple Network Management Protocol

High performance I/O and high capacity file management

● Distributed/parallel file system, ScaTeFS (NEC Scalable Technology File System)

With distributed data servers and distributed meta-data servers, the ScaTeFS can address all kinds of scalability and capacity issues which can show up in the HPC field. This ScaTeFS provides the highest capacity as well as superior single stream I/O performance, and because of the excellent scalability features, it can scale up to huge aggregate performance for parallel I/O from applications. Moreover, caches for data and meta-data reduce data traffic between multiple clients (compute nodes) and I/O servers, such that data access performance for small files and meta-data access performance like file-open or attribute-get are drastically improved. In addition, under a large scale network configuration, the advanced protocol can detect and mitigate congestion, guarantee bandwidth, and control priority of I/O requests. IEEE 802.1 DCB (Data Center Bridging) is supported. Even under high load, a very high I/O performance can be achieved. The ScaTeFS can be configured in a fully redundant way, eliminating all single points of failure for servers, paths, and disks to provide a reliable high performance I/O configuration even for mission critical operations. The concept ensures that the I/O configuration can be easily adapted and enlarged while the system is operating.



Flexible resource management and job scheduling

● Resource management

The NQSII*4 batch system manages the resources of various parts of the configuration to achieve optimal allocation even in very complex and mission critical situations. Client functionality, operation management functionality, and job execution functionality are physically separated, providing a single system image. A unified user interface, simple operation management by the integrated functionalities, and compute resource optimization are provided. Moreover, by simulating the future development of the system load, the scheduling will determine the optimal execution sequence of jobs under the prescribed conditions.

● Job scheduling

The "JobManipulator" is a powerful job scheduler which achieves the maximum system availability by strategic resource management and provides advanced features, such as backfill scheduling, fair-share scheduling, and advance reservation for the support of critical operations. The backfill scheduling enables exclusive resource use by assigning necessary compute resources for a job execution in a planned way. Very detailed scheduling policies can be implemented based on the fair-share scheduling on a user, group, and organization level. The starting time of job execution and necessary resource can be assigned by advance reservation.

*4: Network Queuing System developed by Sterling Software for NASA Ames Research Center

Operation management to reduce work load

● Checkpoint/restart

The SX-ACE supports checkpoint/restart which enables to suspend running jobs and resume them later on. It allows the overtaking for urgent jobs and the split execution of jobs. In a multi-node system, the resource scheduling is tightly integrated with MPI. This can also be used for migrating jobs between nodes.

● Operation management

The SX-ACE is controlled from a workstation by operation management software. It controls the configuration, the operations, and hardware/software exceptions. System power on/off and automatic system stop in case of abnormal environment are possible by connecting with the operation management and environment monitoring device in a facility.

Advanced language processing and software development environment

● Advanced auto-vectorizing and auto-parallelizing compiler

NEC has been providing advanced Fortran/C/C++ compiler for auto-vectorization and auto-parallelization for more than 20 years and has built up huge experience. The compilers for the SX-ACE extract the optimal performance using all the hardware features. The auto-parallelization can be mixed with OpenMP and can be optimized by compiler directives.

● Message passing interface, "MPI"

The MPI implementation of the SX-ACE is utilizing the full functionality of the proprietary interconnect IXS, and it is SMP aware, which means messages on a single node will be exchanged by using the node memory. This way low latency and high throughput data transfer are possible. The MPI implementation supports the latest MPI 3.0 standard and is available for both Fortran and C/C++.

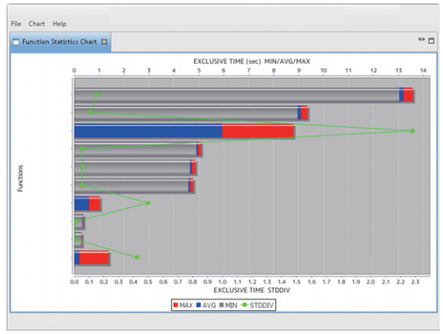
● Data parallel language, "HPF/SX V2"

HPC/SX V2 implementation for the SX-ACE complies with the HPF2.0 basic standard and supports major HPC certified extended specifications and the HPF/JA extended specifications.

Powerful software development aid tools

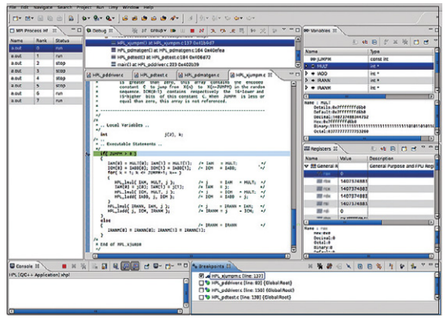
● Performance analysis tool, "NEC Ftrace Viewer"

Ftrace Viewer is a performance analysis tool for Fortran/C/C++ programs. It works for parallel codes which use MPI and OpenMP and displays not only information about the execution time of MPI processes or threads but also information about the communication time between MPI processes in a graphical manner to identify performance of bottlenecks and load imbalance. The Ftrace Viewer supports a wide variety of performance analysis ranging from a single thread program to a large scale parallel program.



● Debugger, "NEC Remote Debugger"

NEC provides a remote debugger which enables interactive debugging from a user terminal. It can handle Fortran/C/C++ and provide various functionalities including debugging of parallel applications based on MPI and shared memory parallelization with OpenMP. The GUI runs on the user's workstation while the application to debug is executed on the SX-ACE.



Mathematical libraries highly tuned for SX series

● Mathematical libraries, "ASL", "ASLSTAT", and "MathKeisan"

NEC has originally developed sophisticated libraries widely used in the field of science and engineering, such as the numerical calculation library, ASL*5, and the statistical calculation library, ASLSTAT*6. Not only Fortran but also C/C++ interfaces are available. In addition, NEC provides a collection of mathematical libraries, MathKeisan, containing optimized versions of public domain libraries, such as BLAS, LAPACK, BLACS, and ScaLAPACK. These libraries are optimized for the SX-ACE.

*5: Advanced Scientific Library *6: Advanced Scientific Library STATistical functions